--Nor are the results improved using more modern damascene processes for the metallization layers of the integrated circuit. Fig. 3A illustrates a current MIM capacitor structure in a integrated circuit manufactured by an exemplary damascene process with the advantage of requiring only one additional masking step. Again, only the details of the metallization layers forming parts of the capacitor structure are described and the capacitor structure which is encircled by a dotted line is shown in greater detail in Fig. 3B.--

A1

Page 5, lines 30 through page 6, line 2, change the paragraph to read:

--The MIM capacitor structure is created by a capacitor dielectric layer 62 on a portion of the M5 metal layer 56 and a capacitor metal layer 63 on the capacitor dielectric layer 62. A metal via 59 connects the capacitor metal layer 63 to the M6 metal layer 60. The details of the capacitor structure is shown in greater detail in Fig. 3B. Note that the M5 metal layer 56 is formed by a Cu layer 56B surrounded by a Ta layer 56A. The capacitor metal layer 63 is a stacked sandwich structure of TiN/AlCu/TiN or Ta/Cu/Ta for the metal layers 63A-63C.--

A2

Page 6, line 22 through page 7, line 14, change these two paragraphs to read:

--The capacitor structure of which the M5 metal layer 86 is a part is encircled by a dotted line and shown in greater detail in Fig. 4B. A first capacitor dielectric layer 91 is placed on a portion of the M5 metal layer 86 and a first metal capacitor plate layer 92 on the dielectric layer 91. Below a portion of the M6 metal layer 90 above the first capacitor dielectric layer 91 and first metal capacitor plate layer 92 is a second metal capacitor plate layer 95 and a second capacitor dielectric layer 93. A metal via 89 separates (and connects) the first metal capacitor plate layer 92 and the second capacitor dielectric layer 93. Fig. 4B illustrates the composition of some of the elements of the capacitor structure in greater detail. The M5 metal layer 86 is formed by a barrier

A3

A3 Cont

metal layer 86A of Ta around a Cu metal layer 86B. The first capacitor dielectric layer 91 (and second capacitor dielectric layer 93) is formed by deposited SiO_2, SiON or SiN. The first metal capacitor plate layer 92 (and second metal capacitor plate layer 95) is a tripartite sandwich structure of metal layers 92A-92C (and 95A-95C) of TiN/AlCu/TiN or Ta/Cu/Ta. The via 89, like the other vias in the metallization interconnection of Fig. 4A is Cu or W.

The MIM capacitor structure forms two capacitors C_1 and C_2 as represented in Fig. 5B. The bottom capacitor C_1 is connected to the M5 metallization layer 86 and the top capacitor C_2 is connected to the M6 metallization layer 90. The via 89, which is actually part of the capacitor structure, connects the two capacitors C_1 and C_2. Structurally it should be noted that in Fig. 4A a right side via 88 connects the M5 metal layer 86 which has a portion covered by the first dielectric layer 91 to the M6 metal layer 90 which has a portion which covers the second metal capacitor plate layer 95. The via 89 connects to M5 and M6 metal layers 86, 90 which are not part of the capacitor structure. To ensure that connection the via 89 is also connected to a via 88 on the left side of the Fig. 4A drawings. Electrically the two capacitors C_1 and C_2 form a circuit shown in Fig. 5B. In other words, if the two capacitors C_1 and C_2 have equal capacitance, the capacitor density is doubled. In the same occupied area, the capacitance is doubled.--

IN THE CLAIMS:

Rewrite claim 1. A markup version is attached and a clean copy follows:

A4

1. (Amended) In an integrated circuit having a substrate and a plurality of stacked metal layers thereover, said metal layers delineated as interconnections for said integrated circuit, a high density capacitor structure between adjacent stacked metal layers comprising